IN THE CLAIMS:

1. (Currently Amended) A phase adjustment circuit ~~for receiving~~ that receives a first pair of clock signals and ~~outputting~~ outputs a second pair of clock signals with phases satisfying a predetermined condition to a central processing unit, comprising:

a clock proliferator ~~for receiving~~ that receives a first clock signal and ~~generating~~ generates a plurality of clock signals therefrom;

a clock selector ~~for receiving~~ that receives said plurality of clock signals from the clock proliferator, ~~selecting~~ selects one of the received plurality of clock signals in accordance with a selection signal, and ~~outputting~~ outputs the selected clock signal; and

a phase difference detector ~~for receiving~~ that receives the selected clock signal and a second clock signal differing in frequency from the first clock signal and the selected clock signal, ~~determining~~ determines whether the phase of the second clock signal and the phase of the selected clock signal satisfy the predetermined condition, and ~~outputting~~ outputs a detection signal indicating whether the predetermined condition is satisfied;

the first clock signal and the second clock signal constituting the first pair of clock signals;

the second clock signal and the selected clock signal constituting the second pair of clock signals.

2. (Original) The phase adjustment circuit of claim 1, wherein the clock proliferators generates the plurality of clock signals by delaying the first clock signal by different amounts.

3. (Original) The phase adjustment circuit of claim 2, wherein the clock proliferators comprises a cascaded plurality of delay elements.

4. (Original) The phase adjustment circuit of claim 1, further comprising:

an external input terminal for input of the selection signal; and

an external output terminal for output of the detection signal.

5. (Currently Amended) The phase adjustment circuit of claim 1, further comprising:

an externally writable register ~~for storing~~ that stores the selection signal and ~~supplying~~ supplies the selection signal to the clock selector; and

an external output terminal for output of the detection signal.

6. (Currently Amended) The phase adjustment circuit of claim 1, wherein the phase difference detector comprises:

a first flip-flop ~~for latching~~ that latches and ~~outputting~~ outputs the state of the second clock signal at rising edges of the selected clock signal;

a second flip-flop ~~for latching~~ that latches and ~~outputting~~ outputs the state of the second clock signal at falling edges of the selected clock signal; and

a logic circuit ~~for performing~~ that performs a logic operation on outputs of the first flip-flop and the second flip-flop, thereby generating the detection signal.

7. (Original) The phase adjustment circuit of claim 6, wherein the first clock signal has a lower frequency than the second clock signal.

8. (Currently Amended) The phase adjustment circuit of claim 1, wherein the phase difference detector comprises:

a first-flop ~~for latching~~ that latches and ~~outputting~~ outputs the state of the selected clock signal at rising edges of the second clock signal;

a second flip-flop ~~for latching~~ that latches and ~~outputting~~ outputs the state of the

second clock signal at falling edges of the selected clock signal; and

a logic circuit ~~for performing~~ that performs a logic operation on outputs of the first flip-flop and the second flip-flop, thereby generating the detection signal.

9. (Original) The phase adjustment circuit of claim 8, wherein the first clock signal has a higher frequency than the second clock signal.

10. (Currently Amended) The phase adjustment circuit of claim 1, further comprising a selection signal generator ~~for receiving~~ that receives the detection signal and ~~generating~~ generates the selection signal.

11. (Original) The phase adjustment circuit of claim 10, wherein the selection signal generator cyclically increases or decreases the selection signal within a certain range of values while the detection signal indicates that the predetermined condition is not satisfied, and holds the selection signal constant while the detection signal indicates that the predetermined condition is satisfied.

12. (Currently Amended) The phase adjustment circuit of claim 10, wherein the selection signal generator comprises:

a register ~~for storing~~ that stores the value of the selection signal;

an adder ~~for adding~~ that adds a fixed value to the value stored in the register to generate a sum value; and

a selector ~~for receiving~~ that receives the value stored in the register and the sum value, ~~selecting~~ selects the value stored in the register when the detection signal indicates that the predetermined condition is satisfied, ~~selecting~~ selects the sum value when the detection signal indicates that the predetermined condition is not satisfied, ~~writing~~ writes the selected value in the register, and ~~supplying~~ supplies the selected value to the clock selector as the selection

signal.

13. (New) The phase adjustment circuit of claim 1, wherein the selected clock signal has a lower frequency than the second clock signal, and the predetermined condition specifies that rising and falling edges of the selected clock signal occur while the second clock signal is high.

14. (New) The phase adjustment circuit of claim 1, wherein the selected clock signal has a higher frequency than the second clock signal, and the predetermined condition specifies that rising and falling edges of the second clock signal occur while the selected clock signal is high.